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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,499	10/16/2003	Chia-Li Chen	BHT-3134-134	5371

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EXAMINER	
GOLDEN, JAMES R	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 10/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,499	CHEN ET AL.	
	Examiner	Art Unit	
	James Golden	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application 10/685499 has a total of 8 claims pending. There is 1 independent claim and 7 dependent claims.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided.

3. The abstract of the disclosure is objected to because “a” (line 5) should be replaced with --an;-- “processes” (line 6) with --that processes;-- “communicates” (line 7) with --that communicates;-- “to” (line 7) with --with;-- “original” (line 10) with --the original;-- “minimized data” with --minimized storage volume;-- “write” (line 11) with --writes;-- “achieve more storage capacity” with --store more data.-- Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because of the following informalities: the first sentence is phrased very awkwardly, perhaps “the” on line 2 should be removed, and “have been” changed to --are;-- other spelling and grammatical errors were noted, but will not be detailed here. The examiner respectfully requests that the applicant review the specification and make appropriate corrections.

Double Patenting

5. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. **Claims 1-2 and 6-8** are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2-6 of copending Application No. 10/685510.

The following table presents a side-by-side comparison of claims 1-2 and 6-8 of the instant application and claims 2-6 of Application No. 10/685510. The differences are presented in bold.

Instant Application	Application No. 10/685510
1. A storage device **available for increasing storage capacity,**	2. A storage device **capable of increasing transmission speed,**
comprising a controller and at least a solid-state storage medium; said controller having a system interface connected to external system end,	mainly comprising a controller and at least a solid-state storage medium; said controller has an internal system interface that may be connected to an external system end,
a microprocessor processing system instructions,	a microprocessor that processes system instructions;
and a memory interface communicating with said solid-state storage medium; wherein:	and a memory interface that communicates with said solid-state storage medium; wherein
said controller has **a data compression module**	said storage device is featured with: **a data compression/decompression module with a data compression mechanism**

between said system interface and said memory interface, and	**is devised in said storage device and**
the data compression module compresses the original data transferred from the system interface in **1/N compression ratio** under the control of the microprocessor and then **stores the compressed data into said solid-state storage medium via said memory interface.**	is designed to compress the raw data transferred via the system interface at an **appropriate compression ratio** into compressed data, **in order to increase data access speed.**
2. A storage device **available for increasing storage capacity** according to claim 1 wherein	3. The storage device **capable of increasing transmission speed** as in claim 2, wherein
said storage device has **a data decompression module between said system interface and said memory interface;**	said data compression/decompression module has **an internal decompression mechanism,**

said decompression module, under the control of said microprocessor, retrieves compressed data stored in said solid-state storage medium and decompresses it to original data to output.	which is triggered by the microprocessor to decompress the compressed data stored in said solid-state storage medium into original raw data and transfer it to the system end.
6. A storage device **available for increasing storage capacity** according to claim 2, wherein said storage device has a first data cache electrically connected to said system interface, said microprocessor, said data compression module and said data decompression module.	4. The storage device **capable of increasing transmission speed** as in claim 2, wherein said storage device has the first data cache, which is wired to said system interface, microprocessor, and data compression/decompression module.
7. A storage device **available for increasing storage capacity** according to claim 2, wherein said controller has a second data cache electrically connected to said	5. The storage device **capable of increasing transmission speed** as in claim 2 wherein said controller has the second data caches, which is wired to said memory

memory interface, said microprocessor, said data compression module and said data decompression module.	interface, microprocessor and data compression/decompression module.
8. A storage device **available for increasing storage capacity** according to claim 2, wherein said data compression module and said data decompression module are **in said controller.**	6. The storage device **capable of increasing transmission speed** as in claim 2, wherein said data compression/ decompression module is embedded in said controller and **between said system interface and said memory interface.**

7. Although the conflicting claims are not identical, they are not patentably distinct from each other.

8. **Claim 2** of the instant application conflicts with claims 2 and 3 of Application No. 10/685510.

- Application No. 10/685510 claims "a storage device capable of increasing transmission speed." This is not a limitation but an inherent effect of the claimed invention, as noted by applicant in the instant application (page 8, lines 3-5). The instant application claims "a storage device available for increasing storage capacity," which is also an inherent effect of the claimed

invention. These effects are unpatentable and therefore cannot be used to differentiate the claims.

- Claim 1 of Application No. 10/685449 does not explicitly claim a decompression module, but claim 2 does; for this reason, claim 1 of the instant application does not conflict with Application No. 10/685510.
- Claim 2 of the instant application allows for either combined or separate compression and decompression modules, while Application No. 10/685510 implies they are combined. The instant application states that "any embodiment implemented with equivalent modifications...(e.g., separate said data compression module and said data decompression module from the controller) shall fall in the scope of the invention" (page 8, lines 17-21), so this is not a patentably distinct difference.
- A "compression module" inherently contains a "compression mechanism," so this mechanism is present in claim 2 of Application No. 10/685510 and claim 1 of the instant application.
- Application No. 10/685510 claims the compression/decompression module is "in said storage device" and the instant application claims the compression module is "between said system interface and said memory interface." The wiring scheme required to connect these components effectively makes "in" and "between" equivalent.
- The instant application claims the data is compressed in a "1/N compression ratio." Application No. 10/685510 claims the data is compressed "at an appropriate compression ratio," which is defined in the specification as "1/N,

wherein 'N' depends on the compression algorithm used..." (page 8, lines 21-22).

- The instant application claims the device "stores the compressed data into said solid-state storage medium via said memory interface." Application No. 10/685510 does not explicitly claim this, but it is a "storage device" and has a solid-state storage medium, so the compressed data must be stored there.
- A "decompression module" inherently contains a "decompression mechanism," so this mechanism is present in claim 3 of Application No. 10/685510 and claim 2 of the instant application.

9. **Claim 6** of the instant application directly conflicts with claim 4 of Application No. 10/685510.

10. **Claim 7** of the instant application directly conflicts with claim 5 of Application No. 10/685510.

11. **Claim 8** of the instant application directly conflicts with claim 6 of Application No. 10/685510.

- As noted above in paragraph 16, "in" and "between" have equivalent meanings because of the wiring scheme required to connect these components effectively.

12. Therefore, it would have been obvious to a person of ordinary skill in the art that claims 1-2 and 6-8 in the instant application and claims 2-6 in Application No. 10/685510 claim the same invention differentiated only by unpatentable inherent effects.

13. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

14. **Claims 3-5** are objected to because of the following informalities. Appropriate correction is required.

15. **Claim 3** recites the limitation "said data decompression module" in line 4. There is insufficient antecedent basis for this limitation in the claim.

16. **Claim 4** recites the limitation "said data decompression module" in line 4. There is insufficient antecedent basis for this limitation in the claim.

17. **Claim 5** recites the limitation "said data decompression module" in line 3. There is insufficient antecedent basis for this limitation in the claim.

18. These objections could be easily overcome by removing the term "said data decompression module" from the claims.

Claim Rejections - 35 USC § 102

19. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

20. **Claims 1-8** are rejected under 35 U.S.C. 102(b) as being anticipated by Pattisam et al. (US 5,357,614).

21. **With respect to claim 1**, Pattisam et al. disclose

- a storage device (20 of Fig. 3) available for increasing storage capacity, comprising

- a controller (20 of Fig. 3) and
- at least a solid-state storage medium (250 of Fig. 3; "solid-state storage" is defined in the specification as "utilizing silicon wafers as the storage media" [page 1, lines 11-12 of instant application]; 250 of Fig. 3 is labeled "compressed data buffers," which are not explicitly recited as solid-state storage media. In column 1, lines 67-68 of Pattisam et al., the "compressed and decompressed data must be buffered through system RAM 12" of prior art. Since the invention of Pattisam et al. is based on this prior art, it would follow that the "compressed data buffers" are memory akin to RAM; RAM uses silicon wafers like the claimed storage media, so 250 is interpreted as the solid-state storage medium);

- said controller having
  - a system interface (206 of Fig. 3) connected to external system end (21 of Fig. 3),
  - a microprocessor processing system instructions (230 of Fig. 3),
  - and a memory interface (213 of Fig. 3) communicating with said solid-state storage medium (250 of Fig. 3) (213 directly linked to, i.e. interfaces with, 250 of Fig. 3);
- wherein: said controller has
  - a data compression module (222 of Fig. 3) between said system interface (206 of Fig. 3) and said memory interface (213 of Fig. 3) (222 shown between in 206 and 213, connected by 212 through 210 and 211 of Fig. 3), and

- the data compression module (222 of Fig. 3) compresses the original data transferred from the system 1/N compression ratio under the control of the microprocessor (230 of Fig. 3) and then stores the compressed data into said solid-state storage medium (250 of Fig. 3) via said memory interface (213 of Fig. 3) (column 12, lines 33-35; although this does not specify a compression ratio of 1/N, the specification of applicant states that " 'N'... may be 2, 3, 4, ..." [page 5, lines 24-25], so as long as there is some data compression by the device of Pattisam et al. it will fit the 1/N requirement).

22. **With respect to claim 2**, Pattisam et al. disclose

- a storage device available for increasing storage capacity according to claim 1 (see above paragraph 21), wherein said storage device has
- a data decompression module (222 of Fig. 3; decompression function detailed in column 17, lines 26-31) between said system interface (206 of Fig. 3) and said memory interface (213 of Fig. 3) (222 shown between in 206 and 213, connected by 212 through 210 and 211 of Fig. 3);
- said decompression module (222 of Fig. 3), under the control of said microprocessor (230 of Fig. 3), retrieves compressed data stored in said solid-state storage medium (250 of Fig. 3) and decompresses it to original data to output (column 17, lines 26-31).

23. **With respect to claim 3**, Pattisam et al. disclose

- a storage device available for increasing storage capacity according to claim 1 (see above paragraph 21), wherein

- said storage device has a first data cache (210 of Fig. 3, labeled as buffer 1; "first data cache" of claim 3 is "used to store data" [page 5, line 16 of specification of the instant application], just as buffer 1 is [column 12, lines 8-13 of Pattisam et al.], so they are therefore functionally equivalent according to the claim limitations) electrically connected to
    - said system interface (206 of Fig. 3),
    - said microprocessor (indirectly through 211 and 216 to 230 of Fig. 3),
    - said data compression module and said data decompression module (through 212 to 222 of Fig. 3).

24. **With respect to claim 4**, Pattisam et al. disclose

- a storage device available for increasing storage capacity according to claim 1 (see above paragraph 21), wherein
- said controller has a second data cache (211 of Fig. 3 , labeled as buffer 2; "second data cache" of claim 4 is "used to store data" [page 5, line 16 of specification of the instant application], just as buffer 2 is [column 12, lines 8-13 of Pattisam et al.], so they are therefore functionally equivalent according to the claim limitations) electrically connected to
    - said memory interface (indirectly through 212 and 222 to 213 of Fig. 3);
    - said microprocessor (indirectly through 216 to 230 of Fig. 3);
    - said data compression module and said data decompression module (through 212 to 222 of Fig. 3).

25. **With respect to claim 5**, Pattisam et al. disclose

- a storage device available for increasing storage capacity according to claim 1 (see above paragraph 21), wherein
- said data compression module and said data decompression module are in said controller (222 inside 20 of Fig. 3).

26. **With respect to claim 6**, Pattisam et al. disclose

- a storage device available for increasing storage capacity according to claim 2 (see above paragraph 22), wherein
- said storage device has a first data cache (210 of Fig. 3; see above paragraph 23 for why this buffer is functionally equivalent to the "first data cache" of claim 6) electrically connected to
    - said system interface (206 of Fig. 3),
    - said microprocessor (indirectly through 211 and 216 to 230 of Fig. 3),
    - said data compression module and said data decompression module (through 212 to 222 of Fig. 3).

27. **With respect to claim 7**, Pattisam et al. disclose

- a storage device available for increasing storage capacity according to claim 2 (see above paragraph 22), wherein
- said controller has a second data cache (211 of Fig. 3; see above paragraph 24 for why this buffer is functionally equivalent to the "second data cache" of claim 7) electrically connected to
    - said memory interface (indirectly through 212 and 222 to 213 of Fig. 3);
    - said microprocessor (indirectly through 216 to 230 of Fig. 3);

- said data compression module and said data decompression module (through 212 to 222 of Fig. 3)

28. **With respect to claim 8**, Pattisam et al. disclose

- a storage device available for increasing storage capacity according to claim 2 (see above paragraph 22), wherein
- said data compression module and said data decompression module are in said controller (222 inside 20 of Fig. 3).

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US 6,847,315 teaches a compressed main memory with multiple caches for the compression controller;
- US 6,446,145 teaches a compression controller with a single cache exclusively for writing to main memory between the system interface and the compression/decompression module;
- US 6,145,069 teaches a compression controller with a single cache between the system interface and compression/decompression module;
- US 2004/0015660 teaches a compression controller with a single cache between a network interface and compression/decompression module.

30. Per the instant office action, claims 1-8 have received a first action on the merits and are the subject of a first action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James R. Golden whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, Donald Sparks, the examiner's supervisor, can be reached on 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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